bq28550 Single Cell Li-Ion Battery Gas Gauge and Protection

Check for Samples: bq28550

FEATURES

- **A Comprehensive Single-Cell Li-Ion Battery Manager Integrates All Essential Functions**
  - **Gas Gauge**
  - **Low-Side N-CH FET Protection Control**
  - **JEITA/Enhanced Charging**
  - **Authentication**
- **Battery Gas Gauge Information**
- **Protection Functions Include:**
  - **Short-Circuit**
  - **Overcurrent Charge and Discharge**
  - **Overvoltage Charge (Overcharge)**
  - **Undervoltage (Over-Discharge)**
  - **Firmware Control of Discharge FET**
- **SHA-1/HMAC Battery Authentication**
- **SMBus Communications Interface**
- **12-pin, 2.5-mm x 4.0-mm SON Package**

APPLICATIONS

- **Tablet PCs**
- **Slates**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

DESCRIPTION

The Texas Instruments bq28550 battery gas gauge provides current and voltage protection, and secure, SHA-1/HMAC authentication for single-cell Li-Ion battery packs. Designed for battery-pack integration, the bq28550 requires host microcontroller firmware support for implementation. A system processor communicates with the bq28550 using one of the serial interface configurations to obtain remaining battery capacity, system run-time predictions, and other critical battery information.

The bq28550 uses an accurate gas gauging algorithm to report the status of the cell. The gauge provides information such as state-of-charge (%), run-time to empty (min.), charge-time to full (min.), battery voltage (V), and pack temperature (°C).

The bq28550 also features integrated support for secure battery-pack authentication, using the SHA-1/HMAC authentication algorithm.

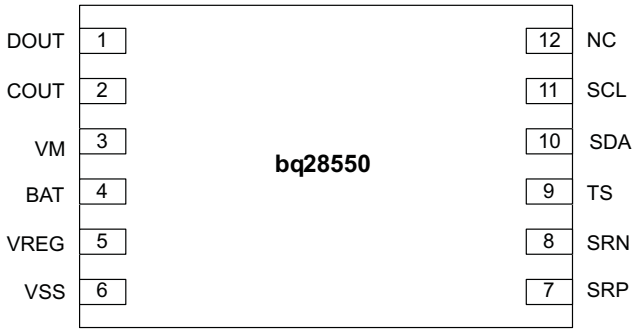

Figure 1. Top View

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION(1)

T_A	PART NUMBER	PACKAGE	TAPE AND REEL QUANTITY
–40°C to 85°C	bq28550DRZR	12-pin, 2.5-mm × 4.0-mm SON	3000
	bq28550DRZT		250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com (www.ti.com).

THERMAL INFORMATION

THERMAL METRIC(1)		bq28550 SON 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	186.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	90.4	
θ_{JB}	Junction-to-board thermal resistance (4)	110.7	
ψ_{JT}	Junction-to-top characterization parameter (5)	96.7	
ψ_{JB}	Junction-to-board characterization parameter (6)	90	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PIN DETAILS

Table 2. Pin Descriptions

PIN NUMBER	PIN NAME	I/O (1)	DESCRIPTION
1	DOUT	IA	The output of gate drive for discharge FET
2	COUT	IA	The output of gate drive for charge FET
3	VM	IA	Analog input pin connected to the PACKN through a 510-Ω resistor. Overcurrent and short-circuit protection circuits use the voltage across VM and VSS to detect if excessive charge or discharge current is flowing through the protection FETs.
4	BAT	IA	Cell voltage measurement input. ADC input. Connect a 0.1-µF ceramic capacitor to VSS.
5	VREG	P	2.5-V output voltage of the internal integrated LDO. Connect a 0.1-µF ceramic capacitor to VSS.
6	VSS	P	Device ground
7	SRP	IA	Analog input pin connected to the internal coulomb counter where SRP is nearest the CELL-connection. Connect to 5-mΩ to 20-mΩ sense resistor.
8	SRN	IA	Analog input pin connected to the internal coulomb counter where SRN is nearest the PACKN connection. Connect to 5-mΩ to 20-mΩ sense resistor.
9	TS	IA	Pack thermistor voltage sense (use 103AT-type thermistor), ADC input
10	SDA	I/O	Serial Data interface for SMBus
11	SCL	I	Serial Clock interface for SMBus

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Table 2. Pin Descriptions (continued)

PIN NUMBER	PIN NAME	I/O (1)	DESCRIPTION
12	NC	I/O	Pull up to VREG with 3.3-K resistor
13	PWPD	I/O	Thermal Pad. Connect to VSS externally on PCB.

FUNCTIONAL BLOCK DIAGRAM

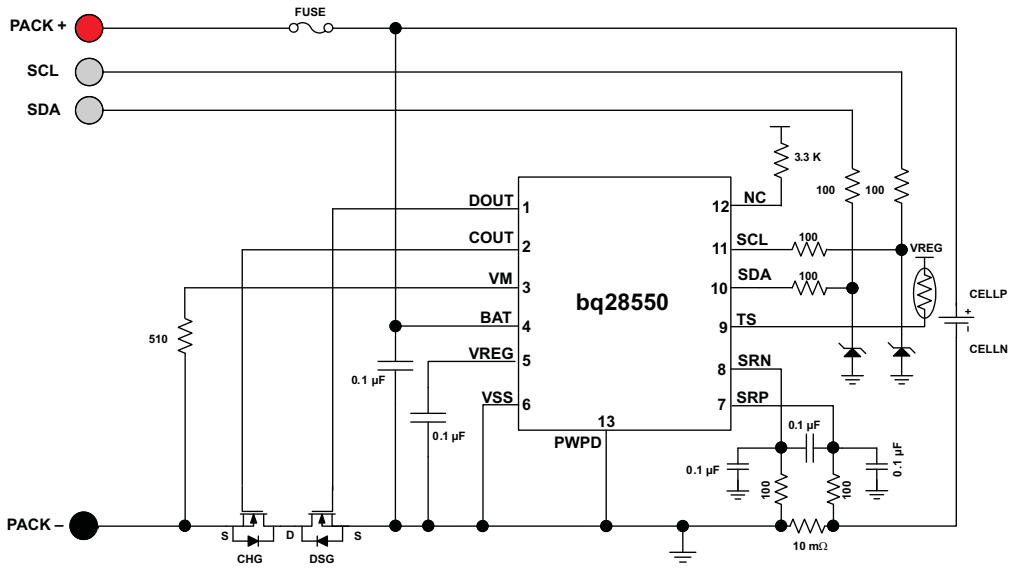

Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to the VSS pin. Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		VALUE	UNIT
V_{BAT}	Regulator input voltage, BAT (Pin 4)	–0.3 V to 6	V
V_{VM}	VM terminal voltage (Pin 3)	V_{BAT} – 32 to V_{BAT} + 0.3	V
V_{COUT}	COUT terminal input voltage (Pin 2)	V_{BAT} – 32 to V_{BAT} + 0.3	V
V_{DOUT}	DOUT terminal input voltage (Pin 1)	V_{SS} – 0.3 to V_{BAT} + 0.3	V
V_{IOD}	All other pins (Pins 5, 7, 8, and 9)	–0.3 to 6	V
V_{SDATA}	SDA (Pin 10)	V_{SS} – 0.3 to V_{BAT} + 0.3	V
V_{SCLK}	SCL (Pin 11)	V_{SS} – 0.3 to V_{BAT} + 0.3	V
ESD	Human body model	±2	kV
ESD	Machine model	±200	V
T_A	Operating free-air temperature range	–40°C to 85	°C
T_{stg}	Storage temperature range	–65°C to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25ºC, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	BAT pin 4 input		2.45	3.6	5.5	V

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RECOMMENDED OPERATING CONDITIONS (continued)

T_A = 25ºC, V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal operating mode	Gas gauge in NORMAL mode. I_{LOAD} > ***Sleep Current***		141		µA
	Low-power (SLEEP)	Gas gauge in SLEEP mode. I_{LOAD} < ***Sleep Current***		70		
	Sleep (FULL SLEEP)	Gas gauge in FULLSLEEP mode. I_{LOAD} < ***Sleep Current***		31		
	Hibernate	Gas gauge in HIBERNATE mode. I_{LOAD} < ***Hibernate Current***		16		
	Shutdown	Gas gauge in SHUTDOWN mode		1		
I_{SS}	Maximum current				20	mA
C_{REG}	Regulator output capacitor		0.1			µF
C_{BAT}	V_{BAT} input filter capacitor			0.1		µF
R_{PACKN}	Resistor from VM to PACKN			510		Ω
$R_{PU_}$	SCL, SDA pull up resistor			3.3		kΩ
$V_{PU_}$	SCL, SDA pull up voltage		2.5		4.2	V
$V_{IL_}$	SDA and SCL Input voltage low	Reference to V_{SS}, V_{BAT} = 2.5 V	–0.5		0.3 V_{BAT}	V
$V_{IH_}$	SDA and SCL Input voltage high	Reference to Vss, V_{BAT} = 2.5 V	0.7 V_{BAT}			V
V_{HYS}	Hysteresis	Reference to V_{SS}, V_{BAT} = 2.5 V, f_{SCL} = 400 kHz (fast mode)	0.05 V_{BAT}			V
$V_{OL_}$	SDA output voltage low	Reference to V_{SS}, V_{BAT} = 2.5 V. I_{OH} = 3 mA (open drain)	0		0.4	V
C_I	Capacitance for each I/O pin	SDA and SCL input capacitance			10	pF
t_{PUCD}	Power Up Communication Delay			250		ms
V_{AI2}	Input voltage range (SRP, SRN)		V_{SS} – 0.25		0.25	V

BATTERY PROTECTION

T_A = –40 to +85ºC, V_{BAT} =1.5 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} =3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{ST}	Minimum operating voltage for 0 V charging	V_{ST} = V_{BAT} – VM			1.2	V
R_{SHORT}	Overcurrent release resistance	V_{BAT} = 4.0 V, VM = 1 V	30	50	100	kΩ
R_{DS}	DS pin pull-down resistance	V_{BAT} = 4.0 V	6.5	13.0	26.0	kΩ
V_{OL1}	COUT Low Level Output voltage (referenced to VM)	I_{OL} = 30 µA, V_{BAT} = 4.5 V		0.4	0.5	V
V_{OH1}	COUT High Level Output voltage (referenced to VM)	I_{OH} = 30 µA, V_{BAT} = 4.0 V	3.4	3.7		V
V_{OL2}	DOUT Low Level Output voltage (referenced to Vss)	I_{OL} = 30 µA, V_{BAT} = 2.0 V		0.2	0.5	V

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BATTERY PROTECTION (continued)

T_A = –40 to +85ºC, V_{BAT} =1.5 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} =3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{OH2}	DOUT High Level Output voltage (referenced to Vss)	I_{OH} = 30 µA, V_{BAT} = 4.0 V	3.4	3.7		V
V_{DET1}	Overcharge detection	T_A = 25˚C detection voltage	4.260	4.280	4.300	V
		T_A = –10 to 60˚C	4.255	4.280	4.305	
		T_A = –40 to 85˚C	4.230	4.280	4.330	
V_{REL1}	Overcharge release voltage	T_A = 25˚C	4.070	4.100	4.130	V
		T_A = –10 to 60˚C	4.055	4.100	4.145	
		T_A = –40 to 85˚C	4.040	4.100	4.160	
t_{DET1}	Overcharge detection delay time	V_{BAT} = 3.5 V ≥ 4.5 V	0.60	1.00	1.50	s
t_{REL1}	Overcharge release delay time	V_{BAT} = 4.5 V ≥ 3.5 V	4.8	8.0	12.0	ms
V_{DET2}	Over-discharge detection voltage	TA = 25˚C	2.265	2.300	2.335	V
		TA = –10 to 60˚C	2.242	2.300	2.358	
		TA = –40 to 85˚C	2.220	2.300	2.380	
t_{DET2}	Over-discharge detection delay time	V_{BAT} = 3.5 V ≥ 2.00 V	14.4	24.0	36.0	ms
t_{REL2}	Over-discharge release delay time	V_{BAT} = 3 V $V_{_}$ = 3 V ≥ 0 V	2.4	4.0	6.0	ms
V_{DET3}	Overcurrent detection voltage on discharge	V_{BAT} = 4 V	0.130	0.150	0.170	V
V_{DET4}	Overcurrent detection voltage on charging	V_{BAT} = 4 V	–0.137	–0.112	–0.087	V
t_{OCD}	Overcurrent detection delay time	V_{BAT} = 3 V $V_{_}$ = 0 V ≥ 1V	7.2	12.0	18.0	ms
t_{OCR}	Overcurrent release delay time	V_{BAT} = 3 V $V_{_}$ = 3 V ≥ 0 V	2.4	4.0	6.0	ms
V_{SHORT}	Short detection voltage	V_{BAT} = 4 V, R_{PACKN} = 510 Ω	V_{BAT} – 1.2	V_{BAT} – 0.9	V_{BAT} – 0.6	V
t_{SHORT}	Short detection delay time	V_{BAT} = 3 V $V_{_}$ = 0V ≥ 3 V	200	400	800	µs

VOLTAGE REGULATOR

T_A = –40 to +85ºC, V_{BAT} =1.5 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} =3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG}	Output voltage	2.7 V < V_{BAT} < 5.5 V, I_{OUT} = 16 mA	2.45	2.50	2.55	V
		2.45 V < V_{BAT} < 2.7 V, I_{OUT} = 3 mA	2.40			
ΔV_{LINE}	Line regulation	2.7 V< V_{BAT} < 5.5 V, I_{OUT} = 16 mA		100	200	mV
ΔV_{LOAD}	Load regulation	V_{REG} = 2.45 V, 100 µA < I_{OUT} < 3 mA		30	50	mV
		V_{BAT} = 2.7 V, 3 mA < I_{OUT} < 16 mA		30	50	
VDO	Dropout voltage	V_{BAT} = 2.45 V, I_{OUT} = 3 mA		30	50	mV
		V_{BAT} = 2.7 V, I_{OUT} = 16 mA		224	290	
$\Delta V_{REG}/\Delta T$	Output voltage temperature coefficient	V_{BAT} = 3.5 V, I_{OUT} = 100 µA		100		ppm/°C
ΔV_{LINE}	Current limit	V_{BAT} = 3.5 V, I_{REG} = 2.0 V	16		130	mA
		V_{BAT} = 3.5 V, I_{REG} = 0 V	10	35	60	
V_{OFF}	Regulator off voltage		7.0	8.0	9.0	V

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VOLTAGE REGULATOR (continued)

T_A = –40 to +85ºC, V_{BAT} =1.5 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} =3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VOFF}	Regulator off voltage delay time	V_{BAT} = 3.6 V → 5.5 V, R_{load} = 100 Ω V_{REG} = 2.5 V → 2.3 V, C_{load} = 0.1 µF, T_A = 25°C		50	100	µs

POWER-ON RESET

T_A = –40 to +85ºC; Typical Values at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at V_{REG}	No external loading on V_{REG}	2.125	2.200	2.275	V
V_{HYS}		No external loading on V_{REG}	75	125	175	mV

INTERNAL TEMPERATURE SENSOR CHARACTERISTICS

T_A = –40 to +85ºC; V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TEMP}	Temperature Sensor Voltage Gain			–2		mV/°C

HIGH FREQUENCY OSCILLATOR

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency			2.097		MHz
$f_{(EIO)}$	Frequency error (1), (2)	T_A = 0°C to 60°C	–2.0	0.38	2.0	%
		T_A = –20°C to 70°C	–3.0	0.38	3.0	%
		T_A = –40°C to 85°C	–4.5	0.38	4.5	%
$t_{(SXO)}$	Start-up time (3)			2.5	5	ms

(1) The frequency error is measured from 2.097 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{CC} = 2.5 V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

LOW FREQUENCY OSCILLATOR

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error (1), (2)	T_A = 0°C to 60°C	–1.5	0.25	1.5	%
		T_A = –20°C to 70°C	–2.5	0.25	2.5	%
		T_A = –40°C to 85°C	–4.0	0.25	4.0	%
$t_{(LSXO)}$	Start-up time (3)				500	µs

(1) The frequency drift is included and measured from the trimmed frequency at V_{CC} = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(SR)}$	Input voltage range, V(SRN) and V(SRP)	VSR = V(SRN) – V(SRP)	–0.125		0.125	V
$t_{CONV(SR)}$	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV

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INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS (continued)

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL	Integral nonlinearity error			±0.007	±0.034	FSR
$Z_{IN(SR)}$	Effective input resistance(1)		2.5			MΩ
$I_{lkg(SR)}$	Input leakage current(1)				0.3	µA

(1) Specified by design. Not production tested.

ADC (TEMPERATURE AND CELL VOLTAGE) CHARACTERISTICS

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(ADC)}$	Input voltage range		–0.2		1	V
$t_{CONV(ADC)}$	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
$Z_{(ADC1)}$	Effective input resistance (TS) (1)		8			MΩ
$Z_{(ADC2)}$	Effective input resistance (BAT) (1)	bq28550 is not measuring cell voltage.	8			MΩ
		bq28550 is measuring cell voltage.		100		kΩ
$I_{lkg(ADC)}$	Input leakage current (1)				0.3	µA

(1) Specified by design. Not production tested.

DATA FLASH MEMORY CHARACTERISTICS

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention (1)		10			Years
	Flash programming write-cycles (1)		20,000			Cycles
$t_{WORDPROG}$	Word programming time (1)				2	ms
I_{CCPROG}	Flash-write supply current (1)			5	10	mA

(1) Specified by design. Not production tested.

SERIAL COMMUNICATION TIMING CHARACTERISTICS

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted). Capacitance on serial interface pins SCL and SDA are 10 pF unless otherwise specified (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		600			ns
$t_{w(L)}$	SCL pulse width (low)		1.3			µs
$t_{su(STA)}$	Setup for repeated start		600			ns

(1) Parameters assured by worst case test program execution in fast mode.

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SERIAL COMMUNICATION TIMING CHARACTERISTICS (continued)

T_A = –40 to +85ºC, V_{BAT} = 2.7 V to 5.5 V; Typical values stated, where T_A = 25ºC and V_{BAT} = 3.6 V (unless otherwise noted). Capacitance on serial interface pins SCL and SDA are 10 pF unless otherwise specified (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		1			µs
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
$t_{(BUF)}$	Bus free time between stop and start		1.3			µs
$f_{(SCL)}$	Clock frequency				100	kHz

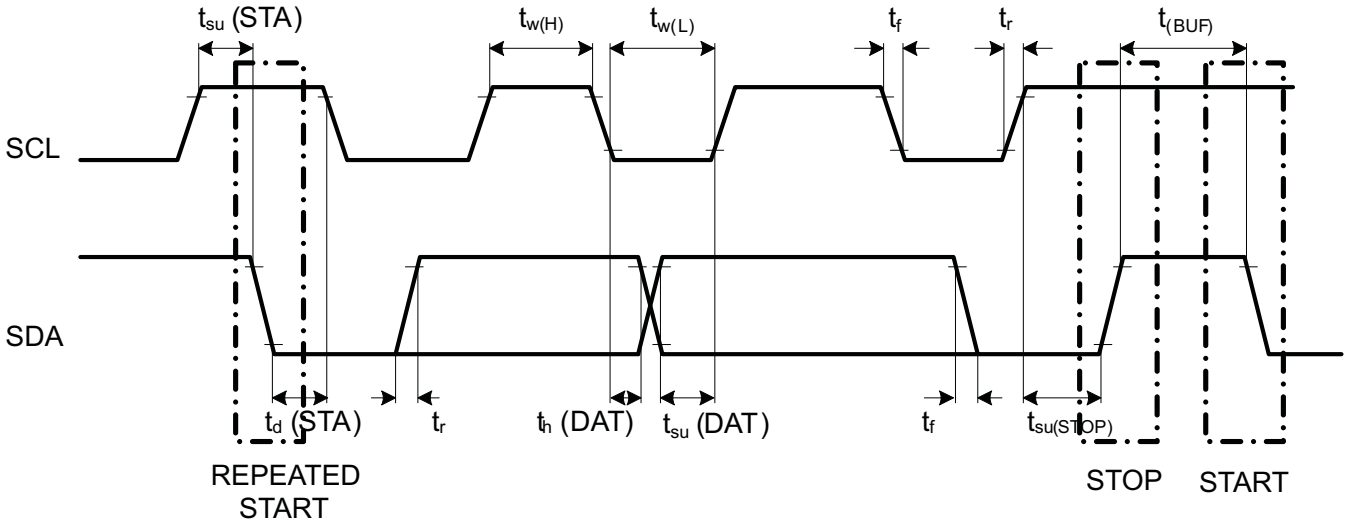

Figure 3. Timing

SERIAL 2-WIRE COMMUNICATION SYSTEM

The 2-wire communication bus supports a slave-only device in a single- or multi-slave configuration with a single- or multi-master configuration. The device can be part of a shared bus by the unique setting of the 7-bit slave address. The 2-wire communication is bi-directional, consisting of a serial data line (SDA) and a clock line (SCL). In receive mode, the SDA terminal operates as an input; whereas, when the device is returning data to the master, the SDA operates as an open drain output with an external resistive pull-up. The master device controls the initiation of the transaction on the bus line.

Data Transfer: Each data bit is transferred during an SCL clock cycle (transition from low-to-high and then high-to-low). The data signal on the SDA (logic level) must be stable during the high period of the SCL clock pulse. A change in the SDA logic when SCL is high is interpreted as a START or STOP control signal. If a transfer is interrupted by a stop condition, the partial byte transmission shall not be latched. Only the prior messages transmitted and acknowledged are latched.

Data Format: The data is an 8-bit format with the most significant bit (MSB) first and the least significant bit (LSB) followed by an Acknowledge bit. If the slave cannot receive or transmit any byte of data until it services a priority interrupt, it can pull the SCL line low to force the master device into wait state. The slave, once ready to resume data transfer, can release the SCL line (get out of wait state).

Bus Idle: The bus is considered idle or busy when no master device has control of this device. The SDA and SCL lines are high when the bus is idle. The appropriate method to go into the STOP condition is to ensure the bus returns to idle state.

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START (S) and STOP (P) Conditions: To initiate communications, the master device transitions the SDA line from high-to-low when the SCL is high. Conversely, to STOP the communication, the SDA goes low-to-high when the SCL is high. To continue communication without termination of one transaction and beginning another, a repeated START (Sr) method can be used without a STOP condition being initiated. These are the only conditions (START or STOP) when SDA transitions when SCL is high.

Acknowledge Bits: An Acknowledge bit (A) is required after each data transfer byte to ensure correct communications. This occurs when the receiving device pulls the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keeps it low until the SCL returns low. There is also a No-Acknowledge bit (N), which occurs when the receiver release the SDA line (high) before the rising edge of acknowledge-related clock pulse, and maintains the SDA line high until SCL returns low. The Acknowledge bit indicates if a successful data transfer has occurred between the master and slave device. Monitoring this bit also indicates an unsuccessful data transfer due to the receiving device being busy or as system fault occurrence.

Communication Format

A **START** command immediately followed by a **STOP** command is an illegal format.

	MSB					
S	Slave Address	R/W	A	Data	A	P

S = START Command

R/W = Read from slave device ("1") or Write to slave device ("0")

A = Acknowledge bit

P = STOP Command

Slave Address = 7-bit address field for register address

DATA = 8-bit data field

PEC = Packet Error Checking

	Slave to Master
	Master to Slave

Communication Format for Multi-Word with Packet Error Checking (PEC)

Table 3. Write Byte with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	PEC	A	P

Table 4. Write Word with PEC

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

Table 5. Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte	A	PEC	A	P

Table 6. Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

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The communication format and protocol complies with SMBus.

GENERAL DESCRIPTION

The bq28550 accurately predicts the battery capacity and other operational characteristics of a single Li-Ion based rechargeable cell, while it also provides a state-of-the-art protection function against short circuit, overcurrent, and overvoltage. It can be integrated by a system processor to provide cell information, such as state-of-charge (SOC), Remaining Capacity, and Full Charge Capacity (FCC).

NOTE

Formatting conventions in this document:

Commands: Italics with parentheses and no breaking spaces; for example, *RemainingCapacity()*.

Data Flash: Italics, bold, and breaking spaces; for example, ***Design Capacity***.

Register Bits and Flags: Brackets only; for example, [TDA]

Data Flash Bits: Italic and bold; for example, ***[NR]***

Modes and States: All capitals; for example, SEALED mode.

DATA ACQUISITION

Cell Voltage

The bq28550 samples the single cell voltage from the BAT input terminal. The cell voltage is sampled and updated every 1 s in normal mode. The VSS ground connection of the bq28550 should be connected to the negative terminal of the sense resistor. This will prevent any error in short circuit and overcurrent measurements across the external CHG and DSG FETs.

Charge Measurement

The device samples the charge into and out of the single cell using a low value sense resistor. The resistor (typically 5 mΩ to 20 mΩ) is connected between SRP and SRN to form a differential input to an integrating ADC (coulomb counter). Charge activity is detected when $V_{SR} = V_{SRP} – V_{SRN}$ is positive, and discharge activity is detected when $V_{SR} = V_{SRP} – V_{SRN}$ is negative. This data is integrated over period of time, using an internal counter and updates Remaining Capacity with charge and discharge amount every 1 s in normal mode.

Current Measurement

The device has a FIFO buffer, which uses the last four coulomb counter readings to calculate the current. The current is updated every 1 s in normal mode.

TEMPERATURE MEASUREMENT AND THE TS INPUT

The bq28550 measures external temperature via the TS pin in order to supply battery temperature status information to the gas gauging algorithm and charger-control sections of the gauge. Alternatively, the gauge can also measure internal temperature via its on-chip temperature sensor. Refer to the ***Pack Configuration[TEMPS]*** control bit.

Regardless of which sensor is used for measurement, a system processor can request the current battery temperature by calling the *Temperature( )* function (see STANDARD DATA COMMANDS for more information). The temperature information is updated every 1 s in normal mode.

The bq28550 external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with R25 = 10 KΩ ± 1% and B25/85 = 3435 KΩ ± 1% (such as Semitec 103AT for measurement). Additional circuit information for connecting this thermistor to the bq28550 is shown in REFERENCE SCHEMATIC.

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OVER-TEMPERATURE INDICATION

Over-Temperature: Charge

If during charging *Temperature()* reaches the threshold of ***OT Chg*** for a period of ***OT Chg Time*** and *AverageCurrent()* > ***Chg Current Threshold***, then the [OC] bit is set based on the charge fault configuration setting of CHG bit in the Control Status Register. When *Temperature()* falls to ***OT Chg Recovery***, the *[OC]* bit is reset.

If ***OT Chg Time*** = 0, the feature is completely disabled.

Over-Temperature: Discharge

If during discharging *Temperature()* reaches the threshold of ***OT Dsg*** for a period of ***OT Dsg Time***, and *AverageCurrent()* ≤ ***–Dsg Current Threshold***, then the [DSGOFFREQ] bit is set. When *Temperature()* falls to ***OT Dsg Recovery***, the *[DSGOFFREQ]* bit is reset.

If *OT Dsg Time* = 0, the feature is completely disabled.

GAS GAUGING

Gas gauging information is accessed through a series of commands called Standard Commands. Further capabilities are provided by the additional Extended Commands set. Both sets of commands, indicated by the general format *Command()*, are used to read and write information contained within the bq28550 control and status registers, as well as their data flash locations. Commands are sent from the system to the gauge using the bq28550's serial interface and can be executed during application development, pack manufacture, or end-equipment operation.

Cell information is stored in the bq28550 non-volatile data flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the bq28550 device's companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known. The bq28550 provides 96 bytes of user-programmable data flash memory, partitioned into three, 32-byte blocks: ***Manufacturer Info Block A***, ***Manufacturer Info Block B***, and ***Manufacturer Info Block C***. For specifics on accessing the data flash, see MANUFACTURER INFORMATION BLOCKS.

The bq28550 device's gas gauging prediction uses a Compensated End of Discharge Voltage (CEDV) method. This algorithm mathematically models the cell voltage as a function of the battery state-of-charge (SOC), temperature, and current. The algorithm also models the battery impedance (Z) as a function of SOC and temperature, with other parameters included in the calculation. The battery voltage model is used to calibrate full charge capacity (FCC), and the compensated battery voltage can be used to indicate low battery voltage or alarm function through firmware settings (Low Battery %, Fully Discharged).

The bq28550 measures discharge activity by monitoring the voltage across a small-value series sense resistor (5 mΩ to 20 mΩ typ) located between the CELL– and the battery's PACKN terminal. This information is used to integrate the battery discharge capacity and to estimate state of charge Q. This is then calculated as a percentage of maximum capacity Qmax to indicate remaining state of charge SOC. The maximum capacity parameter is updated on every full discharge cycle. There are other factors to be considered in estimating remaining state of charge (RSOC), such as battery impedance, temperature, and aging due to number of charge/discharge cycles. The equations used to determine the battery capacity factor these variables in to the calculation based on battery chemistry.

PROTECTION

3.3.1 Overcharge Detector

When charging a battery, if the V_{BAT} voltage becomes greater than the overcharge detection voltage (V_{DET1} = 4.28 V typ) for a period up to the overcharge detection delay time (t_{DET1} = 1.00 s typ), the bq28550 detects the overcharge state of the battery, and the COUT pin transitions to a low level. This prohibits charging the battery by turning off the external charge control N-channel MOSFET.

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In the overcharge state, if a charger is removed and a load is connected, the external charge control MOSFET conducts the load current through its parasitic body diode. If the V_{BAT} voltage becomes lower than the overcharge release voltage (V_{REL1} = 4.1 V typ) for a period up to the overcharge release delay time (t_{REL1} = 8 ms typ), the COUT pin transitions to a high level, enabling charge of the battery by turning on the external charge control N-channel MOSFET.

3.3.2 Over-Discharge Detector

When discharging a battery, if the V_{BAT} voltage becomes lower than the over-discharge detection voltage (V_{DET2} = 2.3 V typ) for a period up to the over-discharge detection delay time (t_{DET2} = 24 ms typ), the bq28550 detects the over-discharge state of the battery, and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

In the over-discharge state, if a charger is connected, the external discharge control MOSFET conducts the charge current through its parasitic body diode. If the V_{BAT} voltage becomes greater than the over-discharge detection voltage (V_{DET2} = 2.3 V typ) for a period up to the overcharge release delay time (t_{REL2} = 4 ms typ), the DOUT pin transitions to a high level enabling discharge of the battery by turning on the external discharge control N-channel MOSFET. After detecting over-discharge, the device stops all operations and enters standby, which reduces the current consumed by the IC to its lowest mode (standby current).

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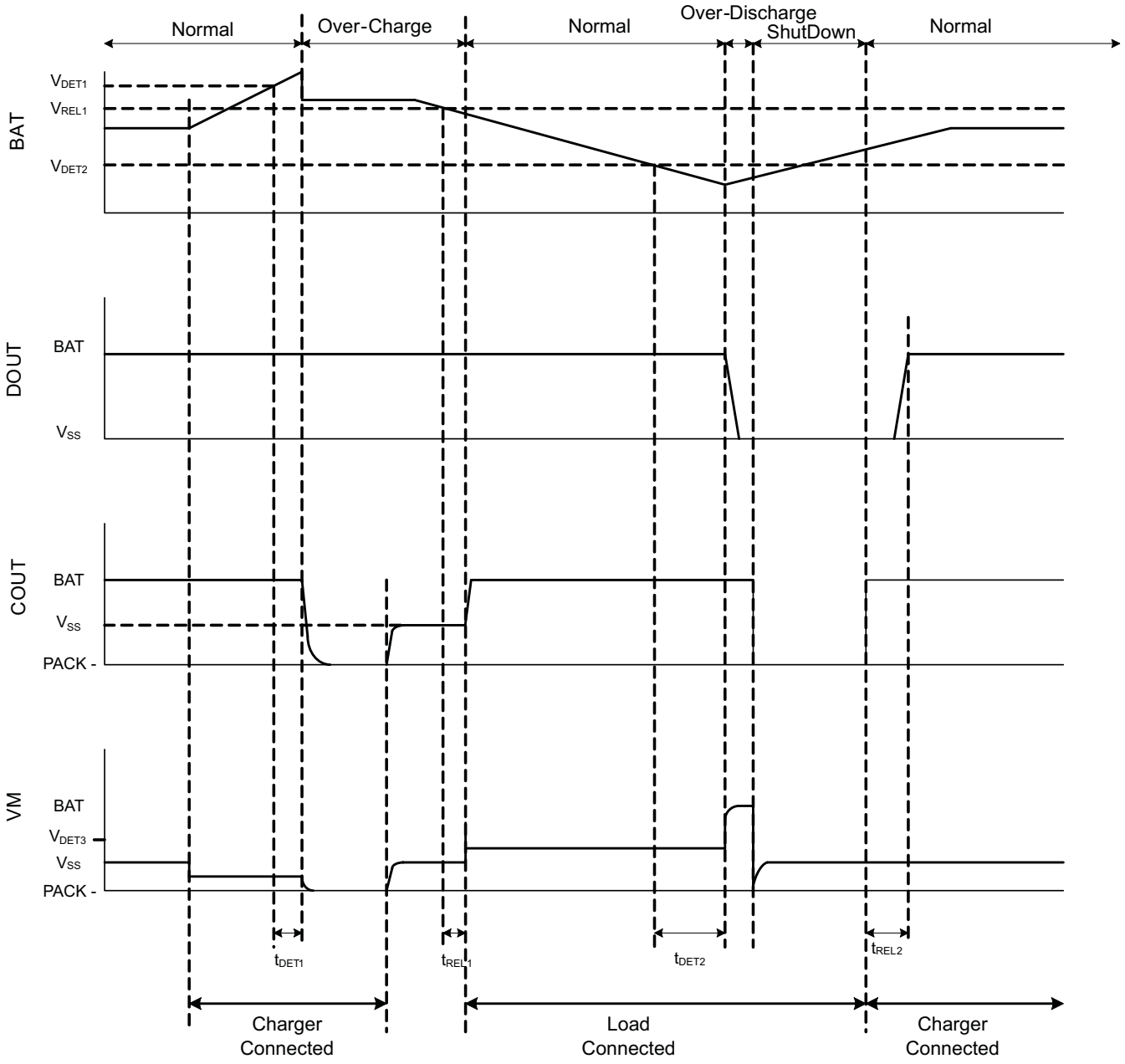

Discharge Overcurrent Detector and Short-Circuit Detector

If the voltage across both protection MOSFETs (V_M – V_{SS}) becomes higher than the discharge overcurrent detection voltage (V_{DET3} = 0.150 V typ) for a period of up to the discharge overcurrent detection delay time (t_{DET3} = 12 ms typ), the bq28550 detects the discharge overcurrent state of the battery and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

Additionally, if the voltage across both protection MOSFETs (V_M – V_{SS}) becomes higher than the short-circuit voltage (V_{SHORT} = V_{BAT} – 0.9 V typ) for a period of up to the discharge short-circuit detection delay time (t_{SHORT} = 400 µs typ), the bq28550 detects short-circuit of the battery and the DOUT pin transitions to a low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

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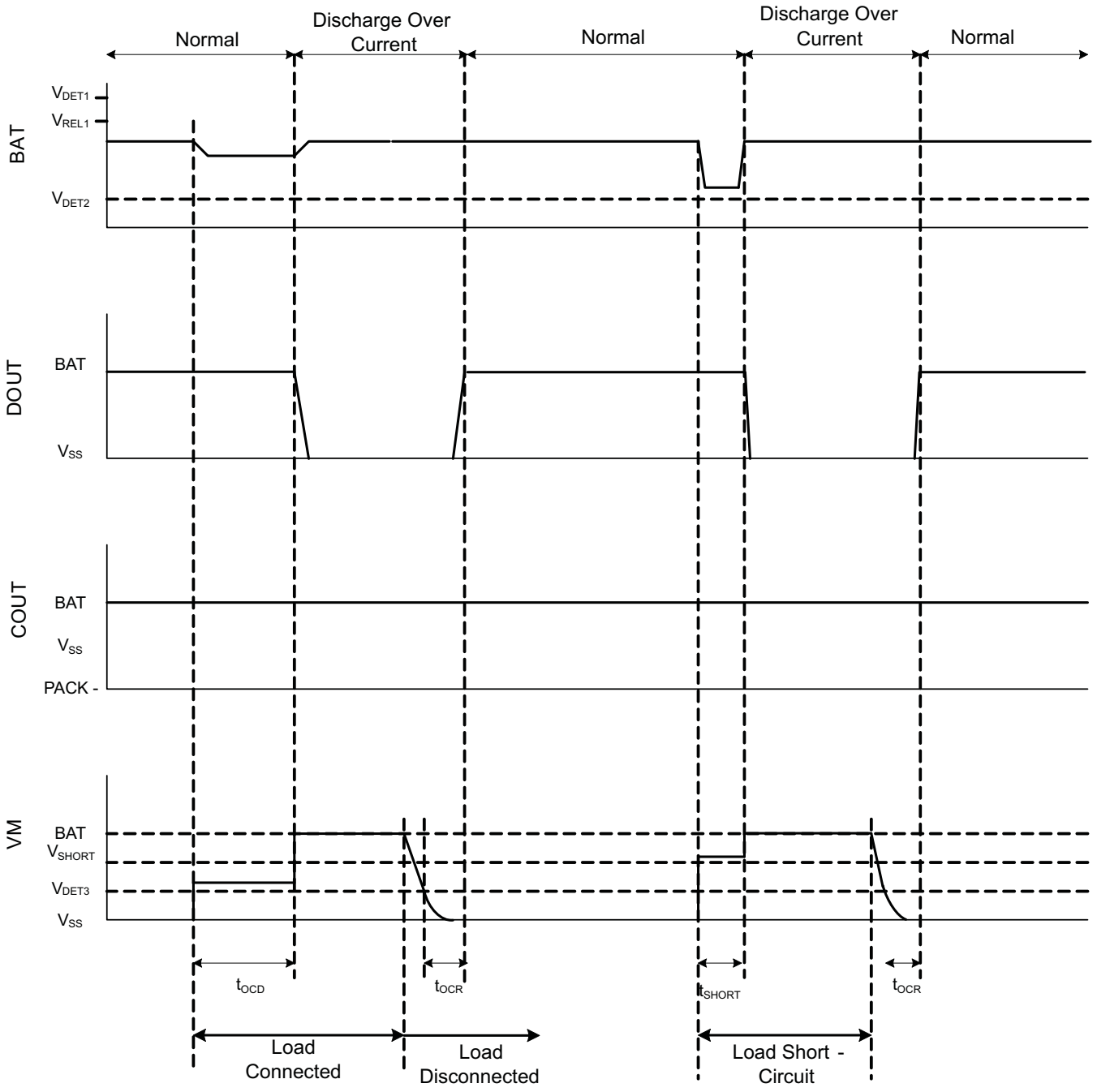
In both the discharge overcurrent and short-circuit states, an internal discharge overcurrent release resistor (20 kΩ typ) is turned on (switched in between VM and VSS), allowing the VM pin to be pulled down to the VSS potential if the load is released. If the $V_M - V_{SS}$ voltage becomes lower than the discharge overcurrent detection voltage (V_{DET3} = 0.150 V typ) for a period up to the discharge overcurrent release delay time (t_{REL3} = 4 ms typ), the discharge overcurrent release resistor is turned off and the DOUT pin transitions to a high level, enabling discharge of the battery by turning on the external discharge control N-channel MOSFET.



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Charge Overcurrent Detector

If the voltage across both protection MOSFETs (V_M – V_{SS}) becomes more negative than the charge overcurrent detection voltage (V_{DET4} = –0.112 V typ) for a period up to the charge overcurrent detection delay time (t_{DET4} = 12 ms typ) due to an abnormal charging current or abnormal charging voltage, the bq28550 detects the overcurrent charge state of the battery and the COUT pin transitions to a low level. This prohibits charging the battery by turning off the external charge control N-channel MOSFET. The bq28550 releases from the charge overcurrent detection state on by detecting the connection of a load for a period up to the overcharge release delay time (t_{REL4} = 4 ms typ).

Table 7. Hardware Control Due to Fault Detection

Fault Condition	DOUT	COUT	Delay (typ)	Comment
Overcharge Voltage Protection	ON	OFF	1 s	Once OVP occurs for longer than the specified duration (1 s typ), the CHG FET is turned OFF and bus communication is NOT valid. The system will support power to the load with current flow through the CHG FET parasitic diode. This can cause the cell to discharge; once the cell voltage reaches the overcharge release voltage for the specified duration (8 ms typ), the CHG FET is turned ON and bus communication is valid.
Overcurrent Protection During Charging	ON	OFF	12 ms	If the cell is being charged with excessive current, the threshold will be based on a hardware limit measurement of –112 mV typ across the CHG + DSG FET (VM – Vss) for a duration longer than 12 ms (typ), the CHG FET is turned OFF and bus communication is *not* valid. This will prevent further charging of the cell. The setting of the CHG bit in the control Status Register is dependent on the OC bit setting in the Charge Fault Register selection. The FET bit in the Control between the charger is removed and cell voltage falls below the threshold for greater than 8 ms (typ). COUT is turned back ON. Once the host MCU takes corrective action OR if the battery charger is removed AND there is a load detected for a period of 4 ms (typ), the CHG FET is turned ON and bus communication is valid.
Over Discharging Voltage Protection	OFF	ON	24 ms	If the cell voltage falls to lower than 2.3 V for a duration of 24 ms (typ), the DSG FET is turned OFF, bus communication is *not* valid. The system requires if charger is connected and cell voltage rises above threshold for greater than 4 ms (typ), DOUT is turned back ON and bus communication is valid.
Overcurrent Protection During Discharging	OFF	ON	12 ms	If the cell is being discharged with excessive current, the threshold will be based on a hardware limit measurement of 150 mV typ across the DSG + CHG FET (VM – Vss) for a duration longer than 12 ms (typ) the DSG FET is turned OFF and bus communication is NOT valid. This will prevent further discharging of the cell, and the DSG bit in the control Status Register will be set. If the drop across the DSG + CHG FET is less than the threshold OR there is *no* load detected for a duration of 4 ms (typ), the DSG FET is turned ON and bus communication is valid.
Short-Circuit Protection	OFF	ON	400 µs	Detection of cell short circuit is measured at VM input. Shorted cell detection is V_{BAT} – 0.9 V for greater than 400 µs at VM terminal, and the DSG FET is turned OFF and bus communication is NOT valid. The DSG bit in the control Status Register will be set. The system will turn the DSG FET ON if the voltage at VM is below 150 mV OR *no* load is detected.

Gas Gauge Control of Discharge DOUT Pin

Firmware Control of DOUT for Protection

The gas gauge firmware can override the hardware-based protection by forcing DOUT low to turn OFF the discharge FET. However, the firmware cannot override the hardware protection to force discharge.

There are three conditions that enable firmware to force DOUT low:

1. The HOST_DISCONNECT (DSG FET OFF) subcommand—This feature is useful for the system to disable the discharge FET from the battery pack if it fails to authenticate.
2. Pack removal detection by SDA and SCL pin falling low for more than 2 seconds—The DOUT pin override condition is released upon detection of PACK insertion.
3. Firmware-based under voltage detection—The DOUT pin is forced low if voltage of the cell falls below the Set Voltage threshold. The DOUT override condition is released when the voltage is above Clear Voltage.

Any one of the above three conditions will force the DOUT pin low. However, all three corresponding release conditions must be satisfied before the DOUT override is returned to hardware-based protection control.

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Zero Voltage Charging

When the cell voltage is 0 V and if the charger voltage is above the minimum operating voltage for 0 V charging (1.2-V max), the COUT output transitions to a high level and charge current can flow.

FET Control Protection

Figure 4 shows an overview of the FET Control Protection operation.

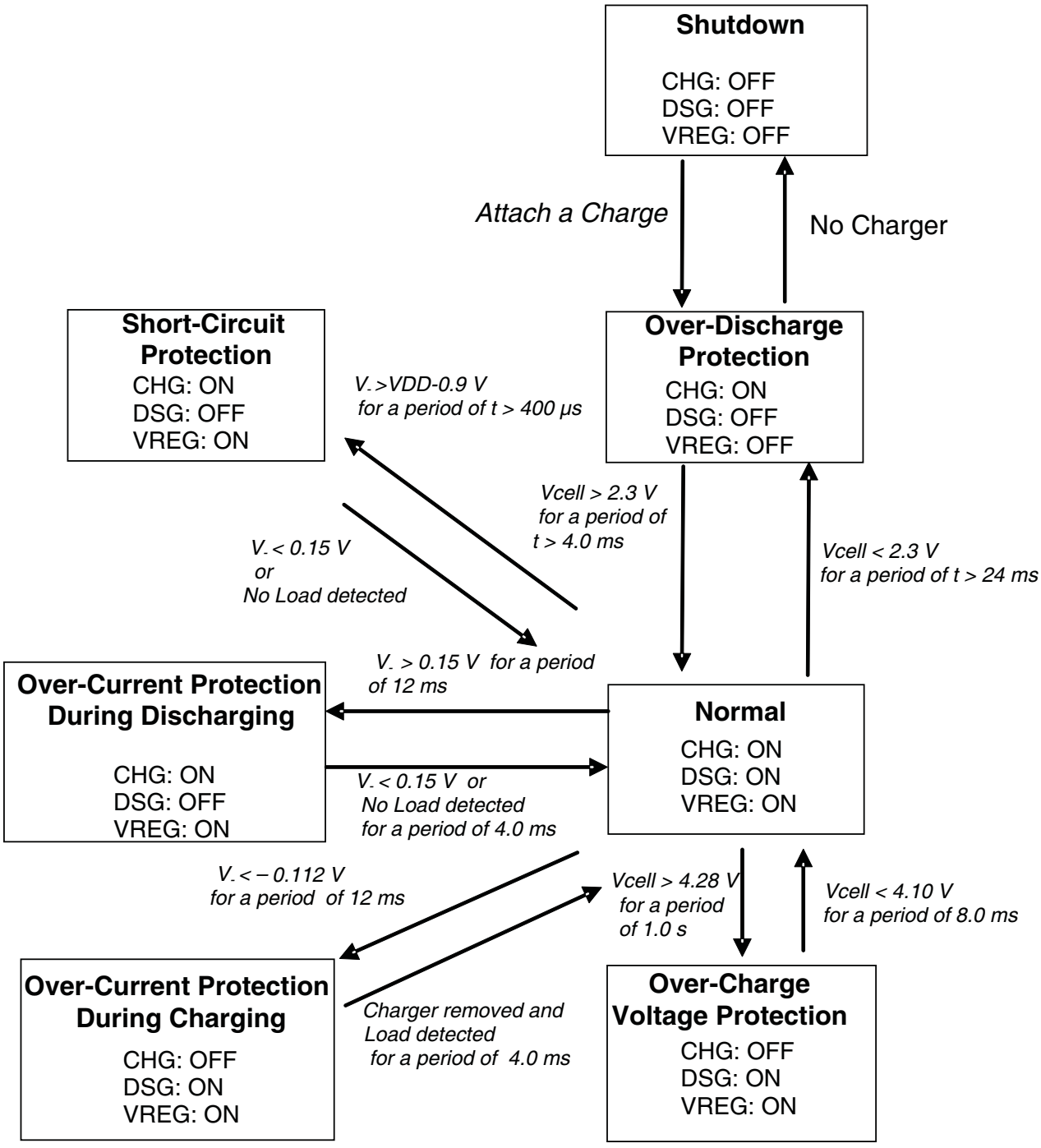

Figure 4. FET Control Protection

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NOTE

When the CHG FET or DSG FET is turned OFF due to fault conditions, bus communication is *not* valid. The bus communication will only be activated by removal of the fault condition (see Table 7).

Regulator

Regulator out voltage is fixed at typically 2.5 V with a minimum output capacitance of 0.1 µF (0.47 µF typ). There is an internal current limit designed for 60 mA (typ) when output is shorted to GND. When VDD is over 8.0 V (typ), the regulator is turned off for the safety of the package dissipation.

DATA COMMANDS

STANDARD DATA COMMANDS

The bq28550 uses the following Command Code. Data RAM is updated and read by the gauge only once per second. Standard commands are accessible in NORMAL operation mode.

Table 8. Standard Commands

Name	Command Code	Min Value	Max Value	Default value	Units	Sealed Access
ManufacturerAccess()	0x00	0x0000	0xffff	—	—	R/W
BatteryMode()	0x03	0x0000	0xe383	—	—	R/W
Temperature()	0x08	0	65535	—	0.1K	R
Voltage()	0x09	0	65535	—	mV	R
Current()	0x0a	–32768	32767	—	mA	R
AverageCurrent()	0x0b	–32768	32767	—	mA	R
MaxError()	0x0c	0	100	—	%	R
RelativeStateOfCharge()	0x0d	0	100	—	%	R
RemainingCapacity()	0x0f	0	65535	—	mAh or 10 mWh	R/W
FullChargeCapacity()	0x10	0	65535	7200	mA	R
ChargingCurrent()	0x14	0	65534	2500	mA	R
ChargingVoltage()	0x15	0	65534	12600	mV	R
BatteryStatus()	0x16	0x0000	0xdbff	—	—	R
CycleCount()	0x17	0	65535	0	—	R/W
DesignCapacity()	0x18	0	65535	7200	mAh	R/W
DesignVoltage()	0x18	0	65535	3600	mV	R/W
SpecificationInfo()	0x1a	0x0000	0xffff	0x0031	—	R/W
ManufactureDate()	0x1b	—	—	0	ASCII	R/W
SerialNumber()	0x1c	0x0000	0xffff	0x0001	—	R/W
ManufacturerName	0x20	—	—	Texas Inst	ASCII	R/W
DeviceName()	0x21	—	—	bq28550	ASCII	R/W
DeviceChemistry()	0x22	—	—	LION	ASCII	R/W
ManufactureData()	0x23	—	—	—	ASCII	R/W
Authenticate()	0x2f	—	—	—	ASCII	R
CellVoltage1()	0x3f	0	65535	—	mV	R
Extended SBS Data Commands						
OperationStatus()	0x54	0x0000	0xffff	—	0xf7f7	R
ChargingStatus()	0x55	0x0000	0xffff	—	—	R
UnSealKey()	0x60	0x00000000	0xffffffff	—	—	R/W

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Table 8. Standard Commands (continued)

Name	Command Code	Min Value	Max Value	Default value	Units	Sealed Access
FullAccessKey()	0x61	0x00000000	0xffffffff	—	—	R/W
AuthenKey0()	0x63	0x00000000	0xffffffff	—	—	R/W
AuthenKey1()	0x64	0x00000000	0xffffffff	—	—	R/W
AuthenKey2()	0x65	0x00000000	0xffffffff	—	—	R/W
AuthenKey3()	0x66	0x00000000	0xffffffff	—	—	R/W
ManufacturerInfo()	0x70	—	—	—	ASCII	R/W
SenseResistor()	0x71	0	65535	—	µΩ	R/W
Temperature()	0x72	0x0000	0xffff	—	—	R
ManufacturerStatus()	0xB1			—	—	R

Run Time to Empty

Battery pack run time to empty can be calculated using the following method—the host system reads and stores the following information during a discharge period and averages the data over a user-determined period of time:

- The DSG bit of the BatteryStatus register is set to ensure DOUT terminal is high (ensure the system is in discharge mode).
- AverageCurrent (mA)
  - Positive value = Charge Current
  - Negative value = Discharge Current
  - One minute rolling average of current value (the user can accumulate this time for improved granularity)
- RemainingCapacity (mAh)

Run Time To Empty = RemainingCapacity (avg mAh) ÷ AverageCurrent (mA). This result will be in hours, and therefore to convert to minutes, divide the results by 60.

Charging Time To Full

This is a read only function that predicts the remaining time until battery reaches full charge in minutes based on Average Current(). The computation accounts for the taper current time extension from the linear TTF computation based on a fixed Average Current() rate of change of accumulation. A value of 65,535 indicates a battery is NOT being charged.

Remaining Capacity Alert

To set a notification when battery capacity is below a pre-determined value, the user can set a Remaining Capacity alarm alert in the system side. The Remaining Capacity value determined by the bq28550 is compared to the user-selected value. If the Remaining Capacity value < the user-selected Remaining Capacity threshold, the host system should instruct the user of what action is needed.

Remaining Time Alert

Similar to the Remaining Capacity notification, a system may require an alarm based on time rather than Remaining Capacity. To set a notification when remaining time to empty is less than the user-set value, the user can set a remaining time to empty alarm alert in the system side. The remaining time to empty value determined by the bq28550 is compared to the user-selected value. If the Remaining Time to Empty value < the user-selected Remaining Time to Empty threshold, the host system should instruct the user of what action to take.

DATA FLASH INTERFACE

ACCESSING THE DATA FLASH

The bq28550 data flash is a non-volatile memory that contains bq28550 initialization, default, cell status, calibration, configuration, and user information. The data flash can be accessed in several different ways, depending on what mode the bq28550 is operating in and what data is being accessed.

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Commonly accessed data flash memory locations, frequently read by a system, are conveniently accessed through specific instructions, as described in DATA COMMANDS. These commands are available when the bq28550 is either in FULL ACCESS, UNSEALED, or SEALED modes.

Most data flash locations, however, are only accessible in FULL ACCESS or UNSEALED mode by using the bq28550 evaluation software or by data flash block transfers. These locations should be optimized and/or fixed during the development and manufacture processes. They become part of a golden image file and can then be written to multiple battery packs. Once established, the values generally remain unchanged during end-equipment operation.

READ-WRITE ACCESS OF DATA FLASH

To read and write commands in data flash, the following method is used:

Command Type	SBS Command	SBS Data	Description
Write Word	0x00	0x1yy	ManufacturerAccess() command to set up the data flash (DF) address in order to write a row (32-byte) of data. Yy = the row number where the target DF address is located.
Read/Write Block	0x2F	32-byte of data	ManufacturerInput() command. Issue this command after setting up the DF address, to read/write the 32-byte data to the DF.

The following is an example procedure to update a parameter in data flash.

1. Identify the physical byte location of the target parameter using the class and subclass ID information. This is typically the subclass ID + Offset.
2. Identify the target row number by truncating the division of the byte location and the row length, e.g. a byte location 27 would be in row: 27 divided by 32 = row number 0.
3. Byte location within the target row is determined by: Byte Index = physical location – (row number * row length)
   Byte Index = 27 – (0 *32) = 27
   The target byte is in row 0 byte 27.
4. Using MAC command 0x1yy, where yy = row number. In this example, the SMBus write command would be 0x100.
5. Read the original target row first through a block read command 0x2F before updating.
6. Store original data in memory array, so the appropriate byte(s) can be updated. SMBus block read cmd = 0x2F, length = 32 byte
7. Store the read data into a memory array (e.g yRowDataArray).
8. Update the target byte (yRowDataArray(27).
9. Write the updated yRowDataArray() array back to the device data flash. This done by repeating Step 4. Issue SMBus block write cmd = 0 × 27, length 32.
10. A read verify is recommended to ensure the data flash has been re-programmed correctly. This is done by repeating Steps 4 and 5 to do a read verify.

Flash Updates

Data flash can only be updated if *Voltage()* ≥ ***Flash Update OK Voltage***. Flash programming current can cause an increase in LDO dropout. The value of ***Flash Update OK Voltage*** should be selected such that the bq28550 V_{CC} voltage does not fall below its minimum of 2.4 V during Flash write operations.

MANUFACTURER INFORMATION BLOCKS

The bq28550 contains 96 bytes of user-programmable data flash storage: ***Manufacturer Info Block A***, ***Manufacturer Info Block B***, ***Manufacturer Info Block C***. The method for accessing these memory locations is slightly different, depending on whether the device is in FULL ACCESS, UNSEALED, or SEALED mode.

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ACCESS MODES

The bq28550 provides three security modes (FULL ACCESS, UNSEALED, and SEALED) that control data flash access permissions according to the content in Table 9. Data flash refers to those data flash locations that are accessible to the user, as specified in .

Table 9. Data Flash Access

Security Mode	SBS Commands	Data Flash	Device Programming
FULL ACCESS	Standard and Extended Commands R/W	R/W	Yes
UNSEALED	Standard and some Extended Commands R/W	R/W	No
SEALED	Standard Commands R/W	None	No

CHARGING AND CHARGE TERMINATION INDICATION

DETECTION CHARGE TERMINATION

For proper bq28550 operation, the cell charging voltage must be specified by the user. The default value for this variable is in the data flash ***Charging Voltage***.

The bq28550 detects charge termination when:

The battery current drops below the ***Taper Current*** for two consecutive ***Current Taper Window*** time periods during charging AND battery voltage is equal to or higher than the ***Charging Voltage*** – ***Taper Voltage***. Full Charge is set when the taper condition is met.

CHARGE SUSPEND

The bq28550 suspends charging when: • Temperature < JT1, OR • Temperature > JT4 in charge-suspend mode, if the [CHGSUSP] bit in OperationConfiguration is set. This will set the charging current to zero and the charging voltage to zero in the Safety Status Register. Also, the CHG bit is reset in ControlStatus register. The bq28550 can indicate to resume charging if: • Temperature ≥ JT1 + Temp Hys, AND • Temperature ≤ JT3 – Temp Hys. On resuming, the bq28550 sets the CHG bit in the ControlStatus Register, and sets ChargingCurrent according to the appropriate charging mode entered. The bq28550 also leaves the charge-suspend mode when the battery is removed in removable battery mode ([NR] = 0).

MANUFACTURER ACCESS(): 0x00/0x01

Issuing a Control() command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The Control() command allows the system to control specific features of the bq28550 during normal operation, and additional features when the device is in access modes (as described in Table 10).

Table 10. Control() Subcommands

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
SET_FULLSLEEP	0x0010	Yes	Set the [FullSleep] bit in Control Status register to 1
SET_HIBERNATE	0x0011	Yes	Forces CONTROL_STATUS [HIBERNATE] to 1
CLEAR_HIBERNATE	0x0012	Yes	Forces CONTROL_STATUS [HIBERNATE] to 0
SET_SHUTDOWN	0x0013	Yes	Forces CONTROL_STATUS [SHUTDOWN] to 1
CLEAR_SHUTDOWN	0x0014	Yes	Forces CONTROL_STATUS [SHUTDOWN] to 0
HOST_DISCONNECT	0x0017	Yes	Forces the DOUT pin low to disable discharge.
HOST_Enable	0x0018	Yes	Forces the DOUT pin high to enable discharge.

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Control Status: 0x0000

Instructs the gas gauge to return status information to Control Status 0x00/0x01. The status word should include the following information.

Table 11. CONTROL STATUS Flags

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RSVD	RSVD	RSVD	RSVD	CCA	BCA	RSVD	RSVD
Low Byte	SHUTRQ	HIBERNATE	FULLSLEEP	SLEEP	DSGOFFREQ	RSVD	CHG	DSG

Low Byte

Bit 0 = DSG FET Status, 1 = Discharging allowed (DSG FET ON), 0 = Discharging NOT allowed (DSG FET Turned OFF)

Bit 1 = CHG FET Status, 1 = Charging allowed (CHG FET ON), 0 = Charging NOT allowed action to be taken by Host MCU

Bit 2 = RSVD (Reserved)

Bit 3 = DSGOFFREQ, DSG FET OFF requested

Bit 4 = SLEEP, Status bit indicating the device is in SLEEP mode. True when set

Bit 5 = FULLSLEEP, Status bit indicating the device is in FULLSLEEP mode. True when set. The state can be detected by monitoring the power used by the device because any communication will automatically clear it.

Bit 6 = HIBERNATE, Status bit indicating a request for entry into HIBERNATE from SLEEP mode has been issued. True when set. Default is 0. Control bit when set will put the device into the lower power state of SLEEP mode. It is not possible to monitor this bit Bit 7 = SHUTRQ, Status bit indicating the gas gauge is enabled to enter SHUTDOWN mode. True when set. Default is 0.

Bit 7 = SHUTRQ, 1 = Shut down requested

High Byte

Bit 0, 1 = RSVD (Reserved)

Bit 2 = BCA = Status bit indicating the device Board Calibration routine is active. Active when set

Bit 3 = CCA = Status bit indicating the device Coulomb Counter Calibration routine is active. Active when set

Bit 4, 5, 6, 7 = RSVD (Reserved).

The following MAC commands are also available.

SET_FULLSLEEP: 0X0010

Instructs the gas gauge to set the FULLSLEEP bit in the Control Status register to 1. This allows the gauge to enter the FULLSLEEP power mode after the transition to SLEEP power state is detected. In FULLSLEEP mode, less power is consumed by disabling an oscillator circuit used by the communication engines. A communication to the device in FULLSLEEP forces it back to SLEEP mode.

SET_HIBERNATE: 0x0011

Instructs the gas gauge to force the CONTROL_STATUS [HIBERNATE] bit to 1. This allows the gauge to enter the HIBERNATE power mode after the transition to SLEEP power state is detected. The [HIBERNATE] bit is automatically cleared upon exiting from HIBERNATE mode.

CLEAR_HIBERNATE: 0x0012

Instructs the gas gauge to force the CONTROL_STATUS [HIBERNATE] bit to 0. This prevents the gauge from entering the HIBERNATE power mode after the transition to SLEEP power state is detected. It can also be used to force the gauge out of HIBERNATE mode.

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SET_SHUTDOWN: 0x0013

Sets the CONTROL_STATUS [SHUTDOWN] bit to 1, enabling the device to enter SHUTDOWN mode if the appropriate conditions are met.

CLEAR_SHUTDOWN: 0X0014

Clears the CONTROL_STATUS [SHUTDOWN] bit to 1, disabling the device from entering SHUTDOWN mode.

DSG FET OFF (HOST_DISCONNECT): 0x0017

Instructs the gas gauge to force the protection DOUT pin to low level. This prohibits discharging the battery by turning off the external discharge control N-channel MOSFET.

DSG FET ON (HOST_CONNECT): 0x0018

Instructs the gas gauge to force the protection DOUT pin to high level. This allows discharging the battery by turning on the external discharge control N-channel MOSFET.

POWER MODES

The bq28550 has four power modes: NORMAL, SLEEP, HIBERNATE, and SHUTDOWN. In NORMAL Mode, the bq28550 is fully powered and can execute any allowable task. In SLEEP Mode, the gas gauge exists in a reduced-power state, periodically taking measurements and performing calculations. In HIBERNATE Mode, the gas gauge is in a low power state, but can be awaken by communication or certain I/O activity. The device enters SHUTDOWN Mode if there is a UVP condition detected or power down of the system.

The relationship between these modes is shown in Figure 5. Details are described in the sections that follow.

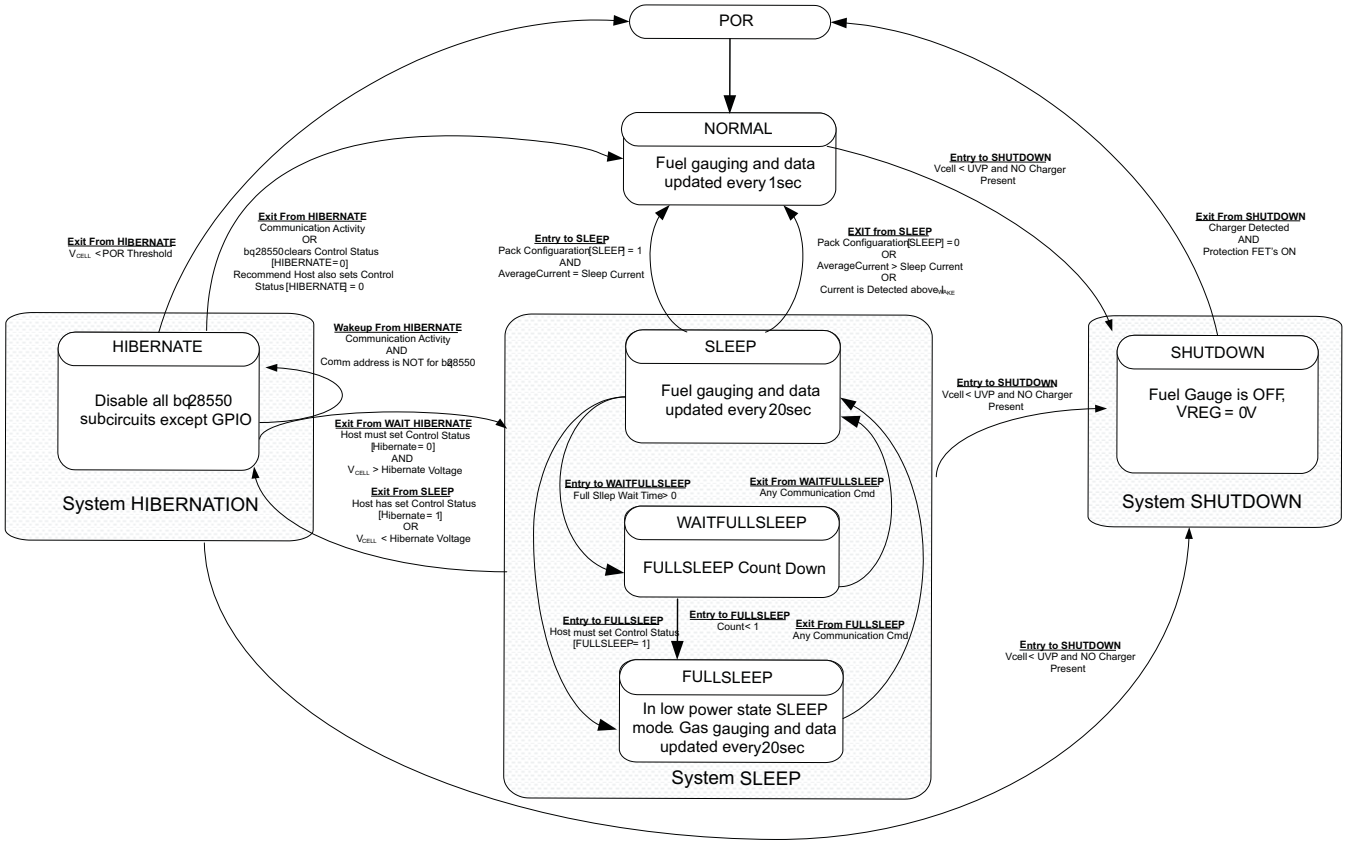

Figure 5. Power Mode Diagram

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NORMAL MODE

The gas gauge is in NORMAL Mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the gauge consumes the most power in NORMAL Mode, the algorithm minimizes the time the gas gauge remains in this mode.

SLEEP MODE

SLEEP Mode is entered automatically if the feature is enabled (***Operation Configuration [SLEEP]***) = 1) and *AverageCurrent()* is below the programmable level ***Sleep Current***. Once entry into SLEEP Mode has been qualified, but prior to entering it, the bq28550 performs an ADC auto-calibration to minimize offset.

While in SLEEP Mode, the gas gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the gas gauge processor is mostly halted in SLEEP Mode.

During SLEEP Mode, the bq28550 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition. The bq28550 exits SLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above ***Sleep Current***, or (2) a current in excess of I_{WAKE} through RSENSE is detected.

FULLSLEEP Mode

FULLSLEEP Mode is entered automatically if the feature is enabled by setting the ***Configuration [FULLSLEEP]*** bit in the Control Status register when the bq28550 is in SLEEP Mode. The gauge exits FULLSLEEP Mode when there is any communication activity. Therefore, the execution of SET_FULLSLEEP sets the ***[FULLSLEEP]*** bit, but EVSW might still display the bit clear. FULLSLEEP Mode can be verified by measuring the current consumption of the gauge. In this mode, the high frequency oscillator is turned off. The power consumption is further reduced in this mode compared to the SLEEP Mode.

FULLSLEEP Mode can also be entered by setting the ***Full Sleep Wait Time*** to be a number larger than 0. FULLSLEEP will be entered when the timer counts down to 0. This feature is disabled when the data flash is set as 0.

During FULLSLEEP Mode, the bq28550 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The bq28550 exits SLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above ***Sleep Current***, or (2) a current in excess of I_{WAKE} through RSENSE is detected.

While in FULLSLEEP Mode, the gas gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the gas gauge processor is mostly halted in SLEEP Mode.

HIBERNATE MODE

HIBERNATE Mode should be used when the host system needs to enter a low-power state, and minimal gauge power consumption is required. This mode is ideal when the host is set to its own HIBERNATE, SHUTDOWN, or OFF modes. The gas gauge can enter HIBERNATE due to either low cell voltage or low load current.

- HIBERNATE due to the load current—If the gas gauge enters HIBERNATE Mode due to the load current, the [HIBERNATE] bit of the CONTROL_STATUS register must be set. The gauge waits to enter HIBERNATE Mode until it has taken a valid OCV measurement and the magnitude of the average cell current has fallen below Hibernate Current.
- HIBERNATE due to the cell voltage—When the cell voltage drops below the Hibernate Voltage and a valid OCV measurement has been taken, the gas gauge enters HIBERNATE Mode. The [HIBERNATE] bit of the CONTROL register has no impact for the gas gauge to enter the HIBERNATE Mode. If the [SHUTDOWN] bit of CONTROL _STATUS is also set.

The gauge will remain in HIBERNATE Mode until communication activity appears on the communication lines. Upon exiting HIBERNATE Mode, the [HIBERNATE] bit of CONTROL_STATUS is cleared.

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Because the gas gauge is dormant in HIBERNATE Mode, the battery should not be charged or discharged in this mode, because any changes in battery charge status will not be measured. If necessary, the host equipment can draw a small current (generally infrequent and less than 1 mA, for purposes of low-level monitoring and updating); however, the corresponding charge drawn from the battery will not be logged by the gauge. Once the gauge exits to NORMAL Mode, the algorithm re-establishes the correct battery capacity.

If a charger is attached, the host should immediately take the gas gauge out of HIBERNATE Mode before beginning to charge the battery.

CAUTION

Charging the battery in HIBERNATE Mode results in a notable gauging error that will take several hours to correct.

SHUTDOWN MODE

The device enters SHUTDOWN Mode if there is a UVP condition detected or power down of the system, and alternatively by setting the SHUTRQ bit to 1, if appropriate conditions are met. The device can also disable SHUTDOWN by using the CLEAR_SHUTDOWN (0x0014) option.

Figure 6 shows an overview of the hardware controlled SHUTDOWN operation.

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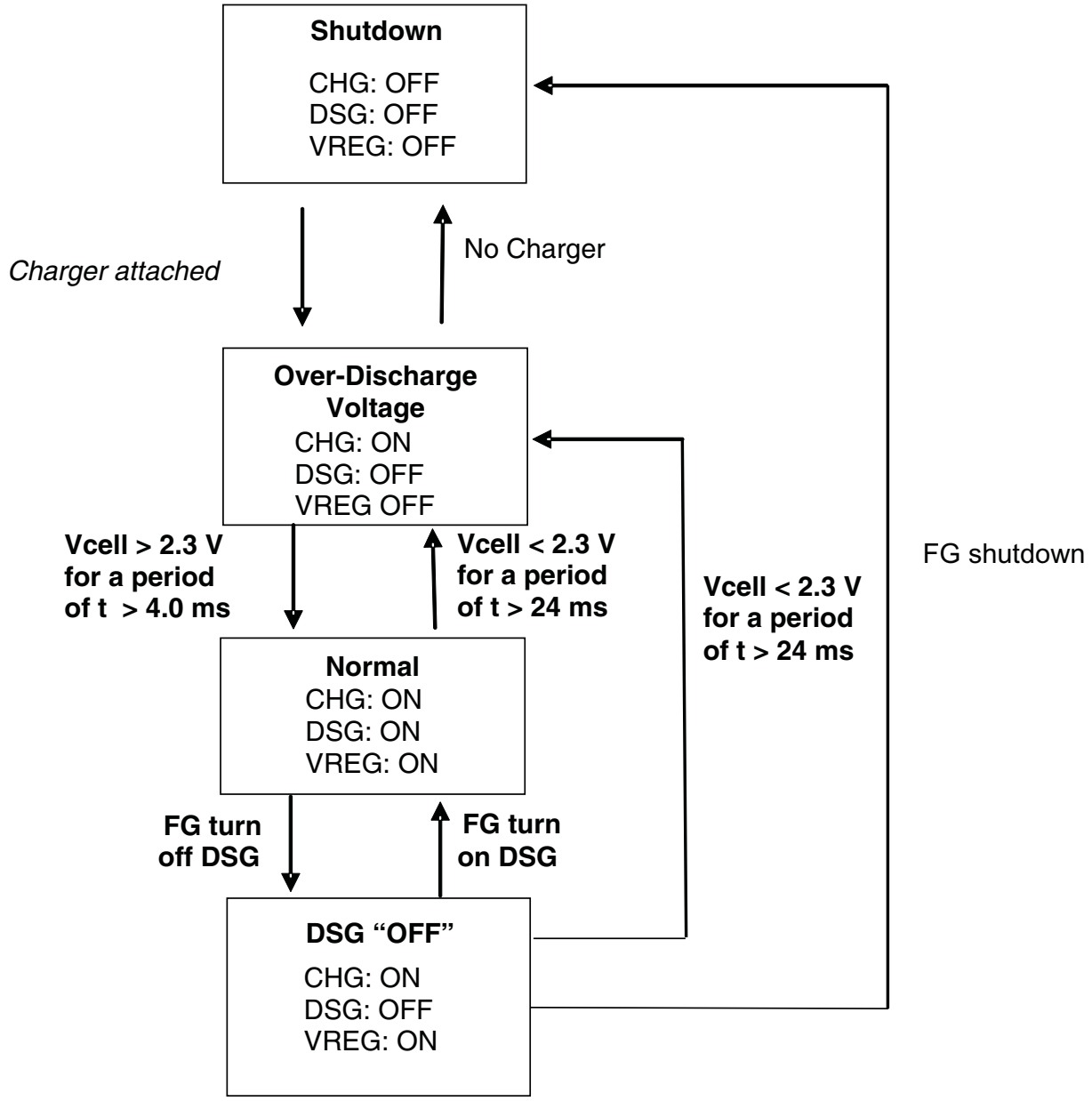

Figure 6. Shutdown Operation

OPERATIONAL MODES

The mode of going from one state to another is as follows, NORMAL → SLEEP → FULLSLEEP; then from FULLSLEEP either HIBERNATE or SHUTDOWN.

Mode	Enter Mode	Exit Mode	Comment
NORMAL	If ALL conditions are satisfied like Average Current, Cell Voltage, and Temperature	Go into other modes like SLEEP, FULLSLEEP, HIBERNATE, or SHUTDOWN mode if conditions are satisfied	In this mode, power consumption is the highest. Measurements are taken and updated every 1 s.

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Mode	Enter Mode	Exit Mode	Comment
SLEEP	SLEEP bit set = 1 in operation register AND AverageCurrent measured is equal to Sleep current value.	Change SLEEP bit = 0 OR AverageCurrent measurement > Sleep current value OR Current detected is above the I_{WAKE} setting.	The data is measured every 20 s to reduce current consumption.
FULLSLEEP	From SLEEP mode if the WAIT_FULLSLEEP wait is programmed, this is the time the system must be in SLEEP mode before it can go to FULLSLEEP mode.	The system exits the FULLSLEEP mode if there are any communication commands set on the bus to the device.	The wait time to enter FULLSLEEP from SLEEP is 1 s to 240 s with the default at 15 s.
HIBERNATION	From FULL SLEEP mode, the system will go into HIBERNATE mode if the load current decreases to programmed value OR if the cell voltage falls below programmed value OR the host sets the command in MAC.	The system exits this mode is the V_{CELL} > programmed threshold OR load current is > programmed threshold OR communication activity on bus line OR host sets the command in MAC.	Enters hibernation if V_{CELL} range is 2.4 V to 3 V with default at 2.55 V. The load current threshold range is 0 to 0.7 A with a default value of 8 mA.
SHUTDOWN	From SLEEP mode, the system will enter this mode if the VCELL < 2.4 V for a period longer than 24 ms and the charger is not attached. The system can also be put in SHUTDOWN mode through MAC.	Exit from this mode if there is bus activity OR the load current detected is > I_{WAKE} OR charger is connected to the system.	In this mode, the VREG and DSG FET are turned OFF and the system will only wake up if the charger is attached on the Pack+, Pack– terminals.

AUTO-CALIBRATION

The bq28550 provides an auto-calibration feature that measures the voltage offset error across SRP and SRN from time-to-time as operating conditions change. It subtracts the resulting offset error from the normal sense resistor voltage, VSR, for maximum measurement accuracy.

Auto-calibration of the ADC begins on entry to SLEEP mode, except if *Temperature()* is ≤ 5°C or *Temperature()* ≥ 45°C.

The gas gauge also performs a single offset when (1) the condition of *AverageCurrent()* ≤ 100 mA and (2) {cell voltage change since last offset calibration ≥ 256 mV} or {temperature change since last offset calibration is greater than 80°C for ≥ 60 s}.

Capacity and current measurements continue at the last measured rate during the offset calibration when these measurements cannot be performed. If the battery voltage drops more than 32 mV during the offset calibration, the load current has likely increased considerably and the offset calibration will be aborted.

COMMUNICATIONS

AUTHENTICATION

The bq28550 can act as a SHA-1/HMAC authentication slave by using its internal engine. Refer to the Application Note SLUA359 for SHA-1/HMAC for information.

By sending a 160-bit SHA-1 challenge message to the bq28550, it causes the gauge to return a 160-bit digest, based upon the challenge message and a hidden, 128-bit plain-text authentication key. If this digest matches an identical one generated by a host or dedicated authentication master, and when operating on the same challenge message and using the same plain text keys, the authentication process is successful.

Key Programming (Data Flash Key)

By default, the bq28550 contains a default plain-text authentication key of 0x0123456789ABCDEFFEDCBA9876543210. This default key is intended for development purposes. It should be changed to a secret key and the part immediately sealed before putting a pack into operation. Once written, a new plain-text key cannot be read again from the gas gauge while in SEALED mode.

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Once the bq28550 is FULL ACCESS, the authentication key can be changed from its default value by writing to the *Authentication()* Extended Data Command locations. A 0x00 is written to *BlockDataControl()* to enable the authentication data commands. The bq28550 is now prepared to receive the 16-byte plain-text key, which must begin at the command location 0x40 and ending at 0x4f. Once written, the key is accepted when a successful checksum for the key has been written to *AuthenticateChecksum()*. The gauge can then be SEALED again.

Key Programming (The Secure Memory Key)

As the name suggests, the bq28550 secure-memory authentication key is stored in the secure memory of the bq28550. If a secure-memory key has been established and Data Flash Key is 0x00000000000000000000000000000000, only this key can be used for authentication challenges (the programmable data flash key is not available). The selected key can only be established/programmed by special arrangements with TI, using TI's *Secure B-to-B Protocol*. The secure-memory key can never be changed or read from the bq28550.

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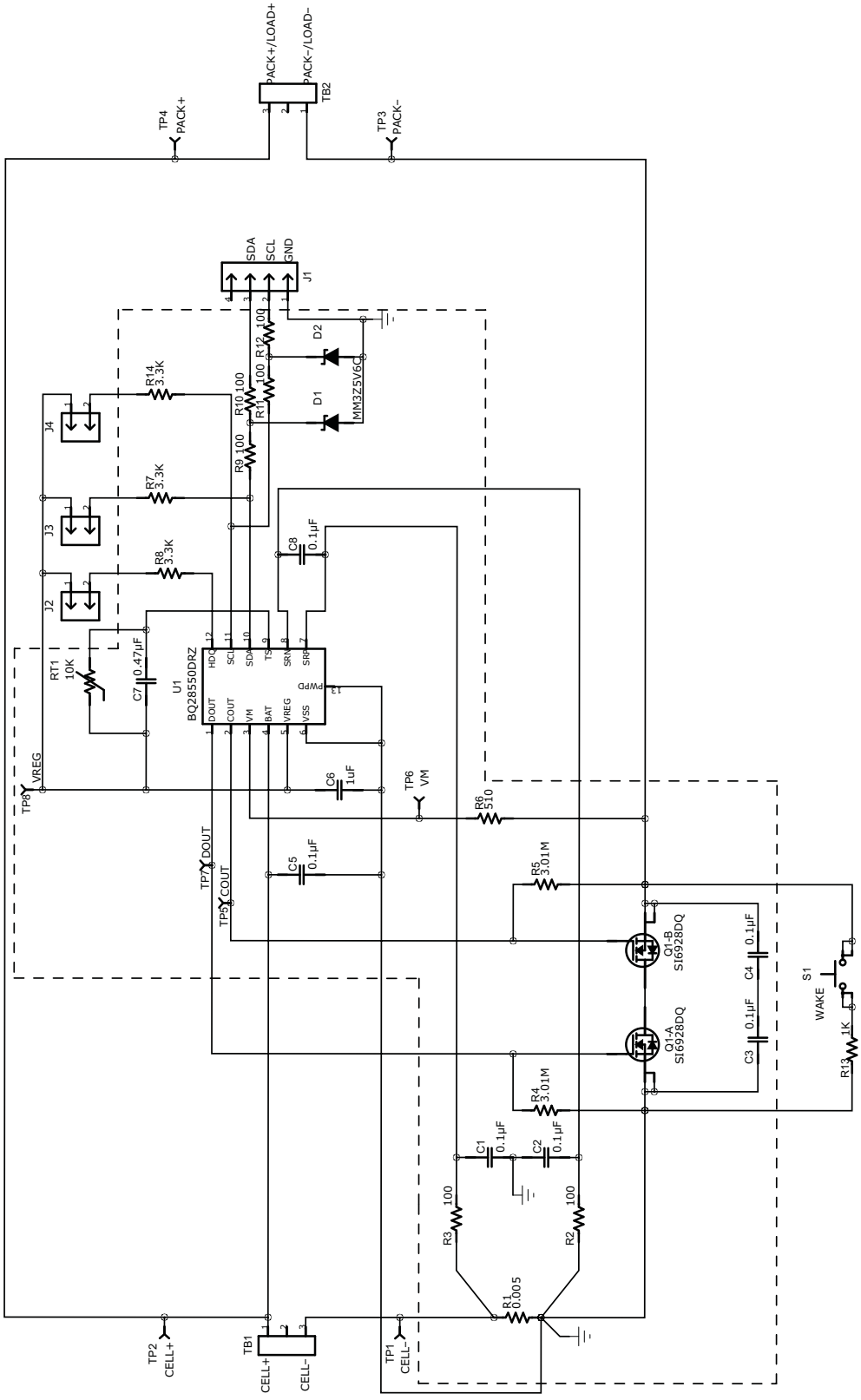
REFERENCE SCHEMATIC

SCHEMATIC



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ28550DRZR	NRND	SON	DRZ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 2855	
BQ28550DRZT	NRND	SON	DRZ	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 2855	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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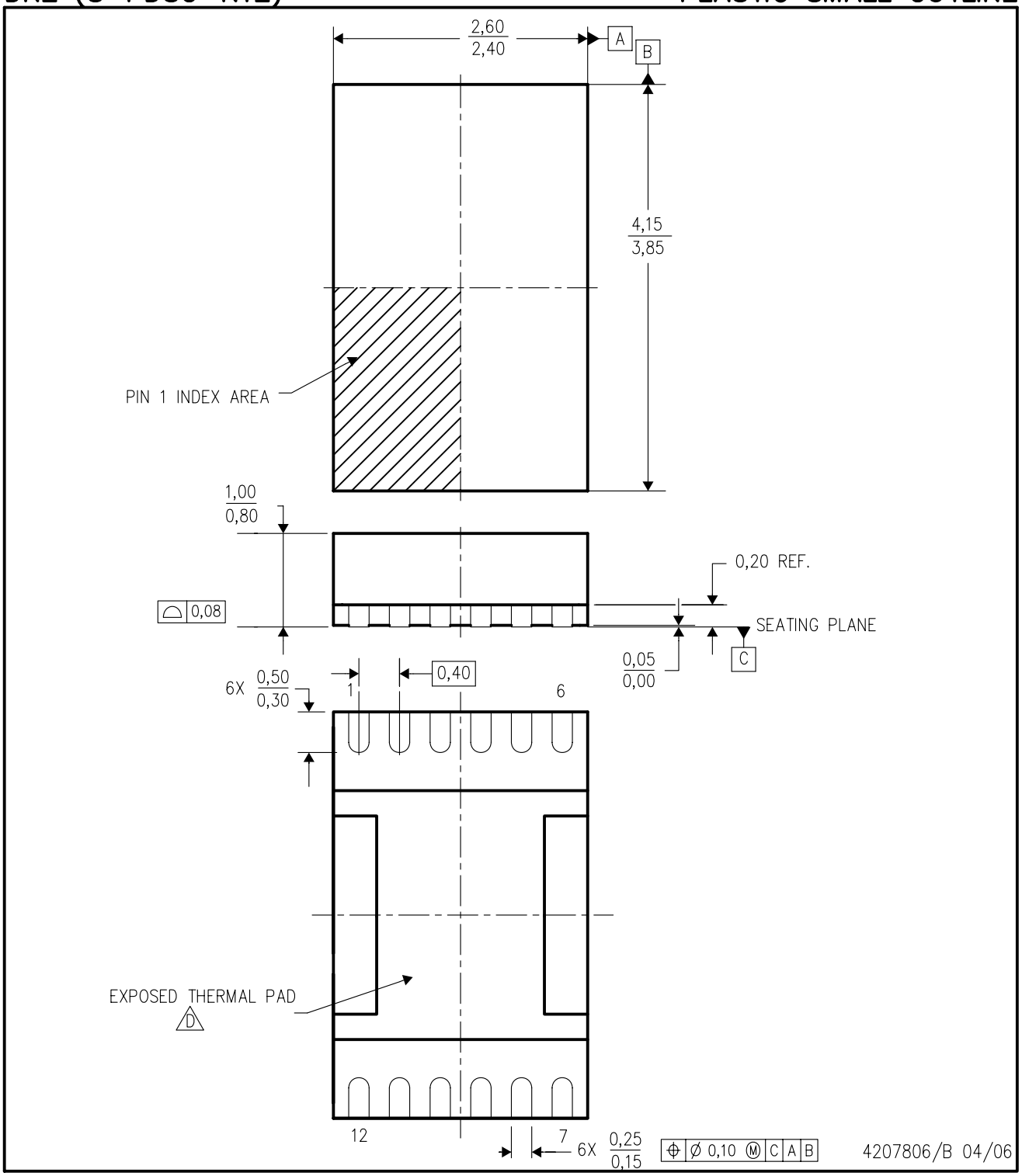
DRZ (S–PDSO–N12) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is lead–free.

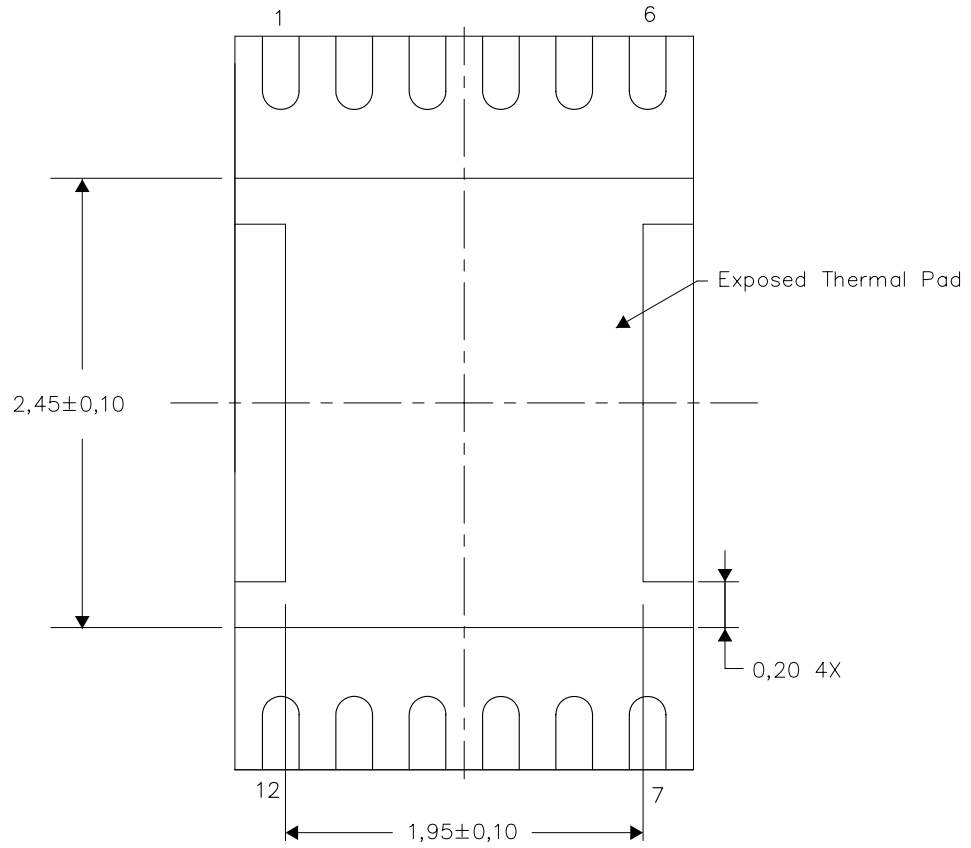
DRZ (R–PDSO–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

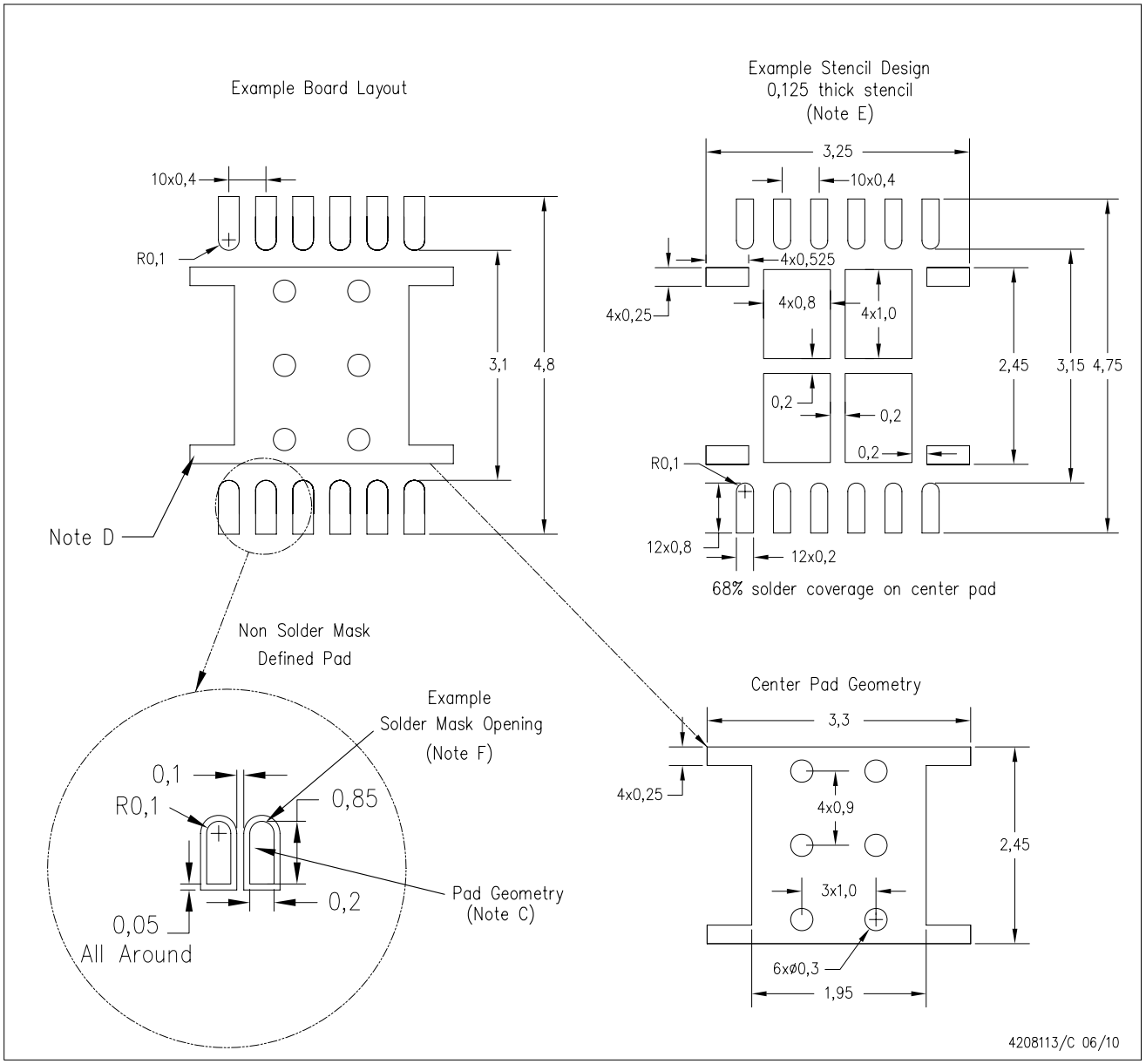


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRZ (S–PDSO–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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